Design Consideration with AP3407/A

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1. Introduction

The AP3407/A is a 1.4MHz fixed frequency, current mode, PWM synchronous buck (step-down) DC-DC converter, capable of driving a 1.2A load with high efficiency, excellent line and load regulation. The device integrates synchronous P-channel and N-channel power MOSFET switches with low on-resistance. It is ideal for powering portable equipment that runs from a single Li-ion battery.

A standard series of inductors are available from several different manufacturers optimized for use with the AP3407/A. This feature greatly simplifies the design of switch-mode power supplies.

The AP3407/A is available in SOT-23-5 package.

2. Function Block Description

The pin configuration and the representative block diagram of the AP3407/A are respectively shown in Figure 1 and Figure 2.

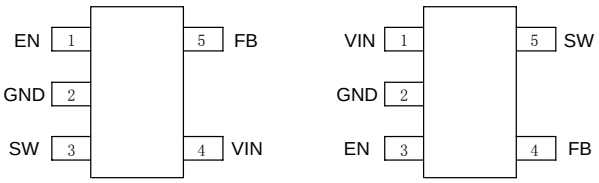

Figure 1. Pin Configuration of AP3407/A (Top View)

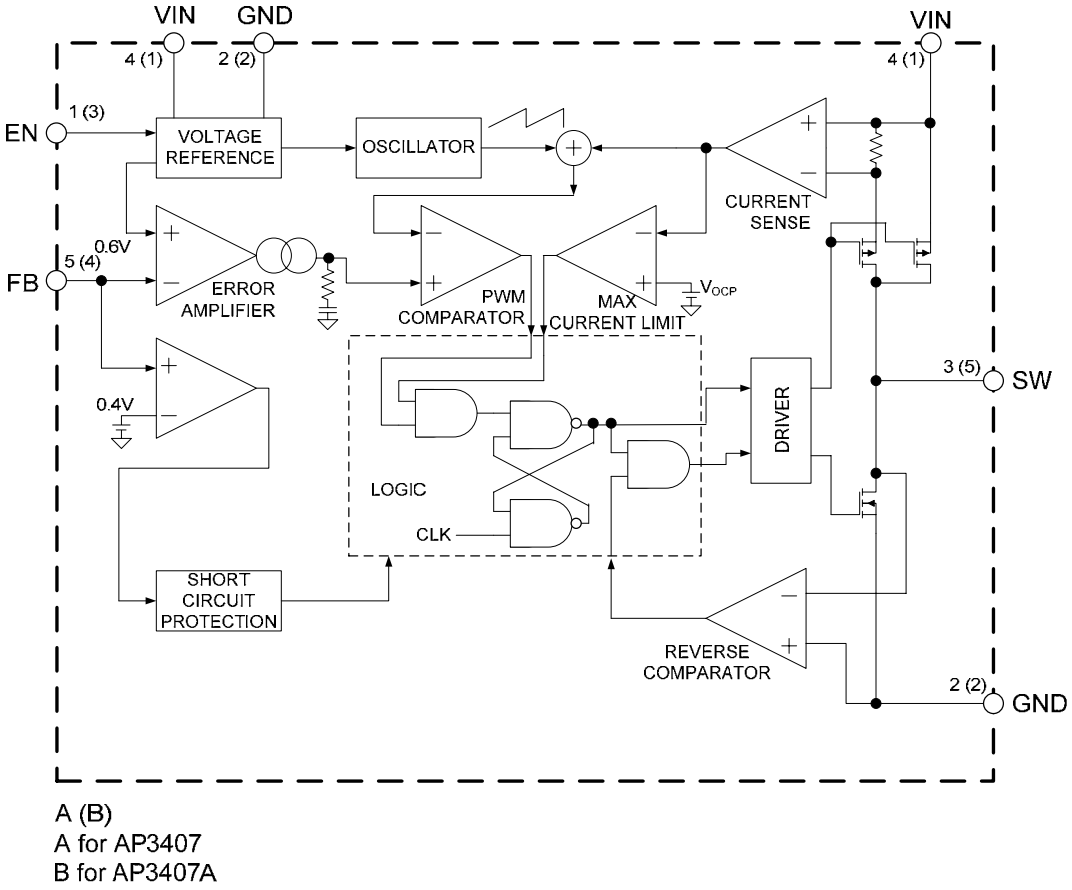

Figure 2. Functional Block Diagram of AP3407/A

3. Operation

The AP3407/A is a synchronous step-down converter operating with typically 1.4MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power-saving moderation (PSM) at operating to light load currents. It is capable of delivering a 1.2A output current over a wide input voltage range from 2.5 to 5.5V.

At the beginning of each cycle initiated by the clock signal (from the internal oscillator), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel MOSFET is exceeded. Then the N-channel synchronous switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again, turning off the N-channel synchronous switch and turning on the P-channel switch (See Figure 2).

Two operational modes are available: PSM and PWM. Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode.

No external Schottky diode is required in practical application. The AP3407/A enters PSM at extremely light load condition. The equivalent switching frequency is reduced to increase the efficiency in PSM.

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases to the maximum. Further reduction of the supply voltage forces the P-channel main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

4. Application

A general AP3407/A application circuit is shown in Figure 3. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once L is chosen, C_{IN} and C_{OUT} can be selected.

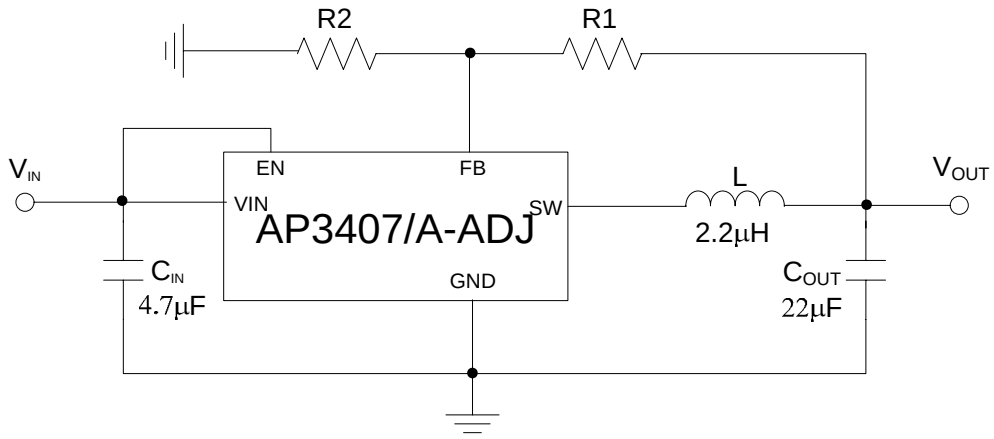

Figure 3. Typical Application of AP3407/A

5. Components Selection

5.1 Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current $\triangle I_L$ decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{f_{OSC} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Accepting larger values of $\triangle I_L$ allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. $\triangle I_L$ typical value is 20% to 40% of output current.

Another important parameter for the inductor is the current rating. Exceeding an inductor's maximum current rating may cause the inductor to saturate and overheat. If inductor value has been selected, the peak inductor current can be calculated as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \frac{V_{IN} - V_{OUT}}{2 \times f_{OSC} \times V_{IN} \times L}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of the I_{PEAK}.

5.2 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes. Place the input capacitor as close as possible to the input pin of the device for best performance. The typical value is about 4.7μF. The X5R or X7R ceramic capacitors have the best temperature and voltage characteristics, which is good for input capacitor.

5.3 Output Capacitor Selection

The output capacitor is the most critical component of a switching regulator, it is used for output filtering and keeping the loop stable. The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\triangle V_{OUT}$) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since $\triangle I_L$ increases with input voltage.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE\ (P\text{-}P)}$ requirement, except for an all ceramic solution. In most applications, a 22μF ceramic capacitor is usually enough for these conditions.

At light load currents, the device operates in PSM mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage V_{OUT}.

5.4 Feedback Divider Resistors

The AP3407/A develops a 0.6V reference voltage between the feedback pin, FB, and the signal ground as shown in Figure 3. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2} \right)$$

Keeping the current small (<40μA) in these resistors maximizes efficiency, but making them too small (<20μA) may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

6. Layout Consideration

PCB layout is very important to the performance of the AP3407/A. The loop which switching current flows through should be kept as short as possible. The external components (especially C_{IN}) should be placed as close to the IC as possible. Therefore use wide and short traces for the main current paths, as indicated in bold in Figure 4.

Try to route the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes

involve a trade-off, but keeping it away from inductor and other noise sources is the more critical of the two. Locate the feedback divider resistor network near the feedback pin with short leads.

Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies: VIN or GND.

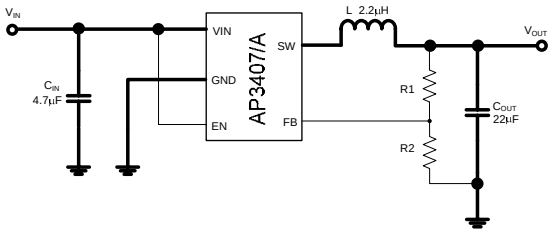

Figure 4. Layout Diagram